FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. ASA-1062	SERIAL NO.
LIST OF DOCUMENTS CITED BY APPLICANT *(Use several sheets if necessary)*		APPLICANT T. SASAKI et al	
		FILING DATE February 13, 2002	GROUP

U.S. PATENT DOCUMENTS

* EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE *(If Appropriate)*
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AL						☐	☐
	AM						☐	☐
	AN						☐	☐
	AO						☐	☐
	AP						☐	☐

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, etc.)*

M-TD	AR		A. Takahashi et al, "Performance and Reliability Driven Clock Scheduling of Sequential Logic Circuits", Proceedings of the ASP-DAC '97, 1997, pp. 37-42.
M-TD	AS		K. Inoue et al, "Schedule-Clock-Tree Routing for Semi-Synchronous Circuits", Technical Report of IEICE, CAD21, 1998, pp. 54-61.
	AT		

EXAMINER	DATE CONSIDERED
	3/19/04

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.